M1CFP4QSFP28CXP

Product Order Number

100G/40G/10G	XenaCompact XenaBay	**C1-M1CFP4QSFP28CXP100** **M1CFP4QSFP28CXP**

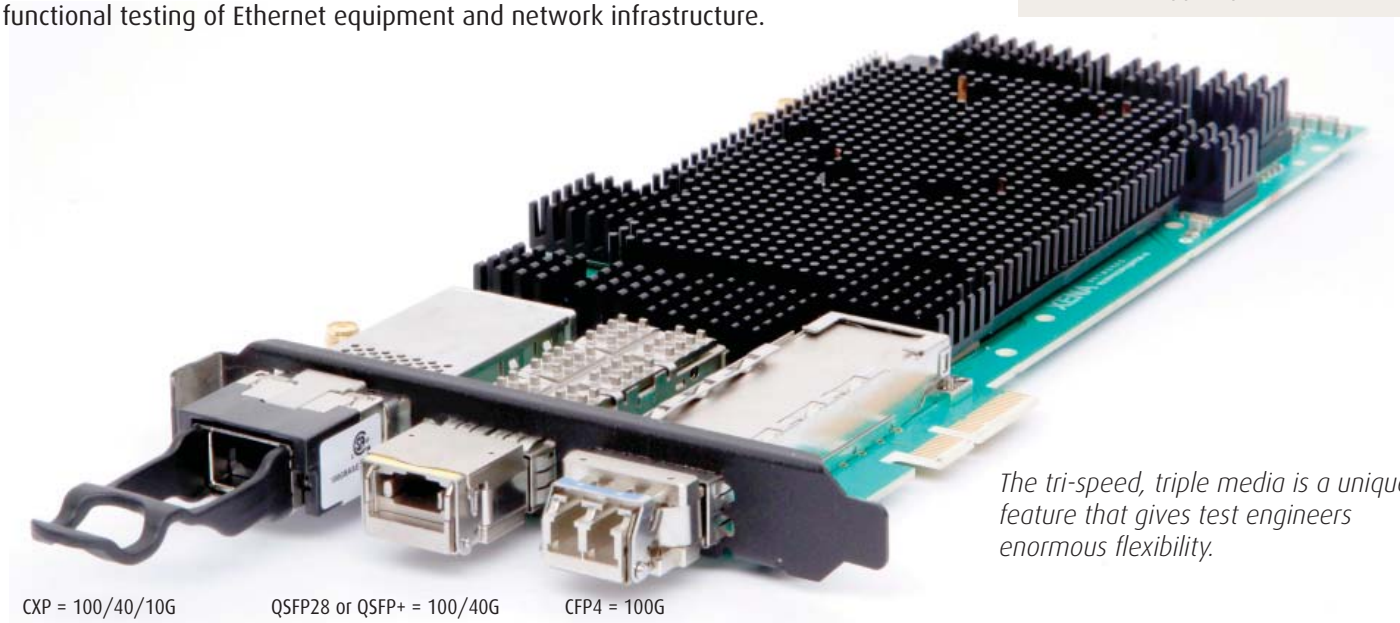
Triple-Media 100/40/10G test module

The M1CFP4QSFP28CXP is a "triple-media" and "tri-speed" 100/40/10G test module for the XenaCompact and XenaBay chassis. This unique test module supports three transceiver form-factors: CFP4 (CAUI-4), QSFP28 (CAUI-4), QSFP+ (CAUI), and CXP (CAUI) and users can choose any one of these transceiver form factor to be active at any time.

When the CXP form-factor is selected, the user can, in addition to a single 100G test port, also use the test module to provide two 40G test ports or eight 10G test ports. This flexibility and price/performance makes it ideal for BERT, load-stress, and functional testing of Ethernet equipment and network infrastructure.

TOP FEATURES

- Tri-speed flexibility
- Triple-media flexibility
- Price/performance
- Ease of use
- Free software (incl. XenaManager-2G, XenaIntegrator, XenaScripting, Xena2544, Xena1564, Xena3918, and Xena2889)
- Free 12-month hardware warranty
- 36 months free software updates
- Free tech support product lifetime



CXP = 100/40/10G QSFP28 or QSFP+ = 100/40G CFP4 = 100G

The tri-speed, triple media is a unique feature that gives test engineers enormous flexibility.

PORT LEVEL FEATURES

Interface category	CXP : 100G, 40G, and 10G Ethernet CFP4/QSFP28 : 100G Ethernet QSFP+ : 40G Ethernet
Number of test ports (software configurable)	CXP : 1 x 100G / 2 x 40G / 8 x 10G CFP4/QSFP28 : 1 x 100G QSFP+ : 1 x 40G
Interface options	CXP : 100GBASE-SR10, 2 x 40GBASE-iSR4 / 8 x 10GBASE-iSR CFP4 : 100GBASE-SR4 , 100GBASE-LR4, 100GBASE-CR4 QSFP28 : 100GBASE-SR4 , 100GBASE-CR4 QSFP+ : 40GBASE-SR4, 40GBASE-LR4, 40GBASE-CR4
Number of transceiver module cages	1 x CXP, 1 x CFP4, 1 x QSFP28/QSFP+ (one cage can be used at a time)
Port statistics [1)]	Link state, FCS errors, pause frames, ARP/PING, error injections, training packet All traffic: RX and TX Mbit/s, packets/s, packets, bytes Traffic w/o test payload: RX and TX Mbit/s, packets/s, packets, bytes
Adjustable Inter Frame Gap (IFG)	Configurable from 16 to 56 bytes, default is 20B (12B IFG + 8B preamble)
Transmit line rate adjustment	Ability to adjust the effective line rate by forcing idle gaps equivalent to -1000 ppm (increments of 10 ppm)
Transmit line clock adjustment	From -400 to 400 ppm in steps of 0.001 ppm (shared across all ports)
ARP/PING	Supported (configurable IP and MAC address per port)
Field upgradeable	System is fully field upgradeable to product releases (FPGA images and Software)
Tx disable	Enable/disable of optical laser or copper link
IGMPv2 multicast join/leave	IGMPv2 continuous multicast join, with configurable repeat interval
Histogram statistics [1)]	Two real-time histograms per port. Each histogram can measure one of RX/TX packet length, IFG, or Latency distribution for all traffic, a specific stream, or a filter
Loopback modes	• L1RX2TX – RX-to-TX, transmit byte-by-byte copy of the incoming packet • L2RX2TX – RX-to-TX, swap source and destination MAC addresses (**only at 10G*) • L3RX2TX – RX-to-TX, swap source and destination MAC addresses and IP addresses (**only at 10G*) • TXON2RX – TX-to-RX, packet is also transmitted from the port • TXOFF2RX – TX-to-RX, port's transmitter is idle • Port-to-port – Inline loop mode where all traffic is looped 100% transparent at L1
Oscillator characteristics	• Initial Accuracy is 3 ppm • Frequency drift over 1st year: +/- 3 ppm (over 15 years: +/- 15 ppm) • Temperature Stability: +/- 20 ppm (Total Stability is +/- 35 ppm)

BETA Version

40G FRAMED PRBS AND PCS LAYERS

Payload Test pattern	PRBS 2^31
Error Injection	Manual single shot bit-errors or bursts, automatic continuous error injection
Frame size and header	Fixed size from 56 to 9200 bytes, any layer 2/3/4 frame header
Alarms	Pattern loss, bit-error rate threshold
Error analysis	bit-errors: seconds, count, rate mismatch '0' / '1': seconds, count, rate logging and analysis of bit-error event timing
PCS virtual lane configuration	User defined skew insertion per Tx virtual lane, and user defined virtual lane to SerDes mapping for testing of the Rx PCS virtual lane re-order function.
PCS virtual lane statistics	Relative virtual lane skew measurement (up to 2048 bits), sync header and PCS lane marker error counters, indicators for loss of sync header and lane marker, BIP8 errors

TRANSMIT ENGINES

Number of transmit streams per port	64 (wire-speed)
	Each stream can generate millions of traffic flows through the use of field modifiers
Test payload insertion per stream	Wire-speed packet generation with timestamps, sequence numbers, and data integrity signature optionally inserted into each packet.
Stream statistics [1)]	TX Mbit/s, packets/s, packets, bytes, FCS error, Pause
Bandwidth profiles	Burst size and density can be specified. Uniform and bursty bandwidth profile streams can be interleaved
Field modifiers	16-bit header field modifiers with inc, dec, or random mode. Each modifier has configurable bit-mask, repetition, min, max, and step parameters. 2 modifiers per stream
Packet length controls	Fixed, random, butterfly, and incrementing packet length distributions from 56 to 9200 bytes
Packet payloads	Repeated user specified 1 to 18B pattern, a 8-bit incrementing pattern
Error generation	Undersize length (56B min) and oversize length (9200 max.) packet lengths, injection of sequence, misorder, payload integrity, and FCS errors
TX packet header support and RX autodecodes	Ethernet, Ethernet II, VLAN, ARP, IPv4, IPv6, UDP, TCP, LLC, SNAP, GTP, ICMP, RTP, RTCP, STP, MPLS, PBB, or fully specified by user
Packet scheduling modes	• Normal (stream interleaved mode) – standard scheduling mode, precise rates, minor variation in packet inter-frame gap. • Strict Uniform – new scheduling mode, with 100% uniform packet inter-frame gap, minor deviation from configured rates • Sequential packet scheduling (sequential stream scheduling). Streams are scheduled continuously in sequential order, with configurable number of packets per stream

RECEIVE ENGINE

Number of traceable Rx streams per port	480 (wire-speed)
Automatic detection of test payload for received packets	Real-time reporting of statistics and latency, loss, payload integrity, sequence error, and misorder error checking
Jitter measurement	Jitter (Packet Delay Variation) measurements compliant to MEF10 standard with 8 ns accuracy
Stream statistics [1)]	• RX Mbit/s, packets/s, packets, bytes. • Loss, payload integrity errors, sequence errors, misorder errors • Min latency, max latency, average latency • Min jitter, max jitter, average jitter
Latency measurements accuracy	±16 ns
Latency measurement resolution	8 ns *(Latency measurements can calibrate and remove latency from transceiver modules)*
Number of filters:	• 4 x 64-bit user-definable match-term patterns with mask, and offset • 4 x frame length comparator terms (longer, shorter) • 4 x user-defined filters expressed from AND/OR'ing of the match and length terms.
Filter statistics [1)]	Per filter: RX Mbit/s, packets/s, packets, bytes.

ADVANCED TIMING FEATURES

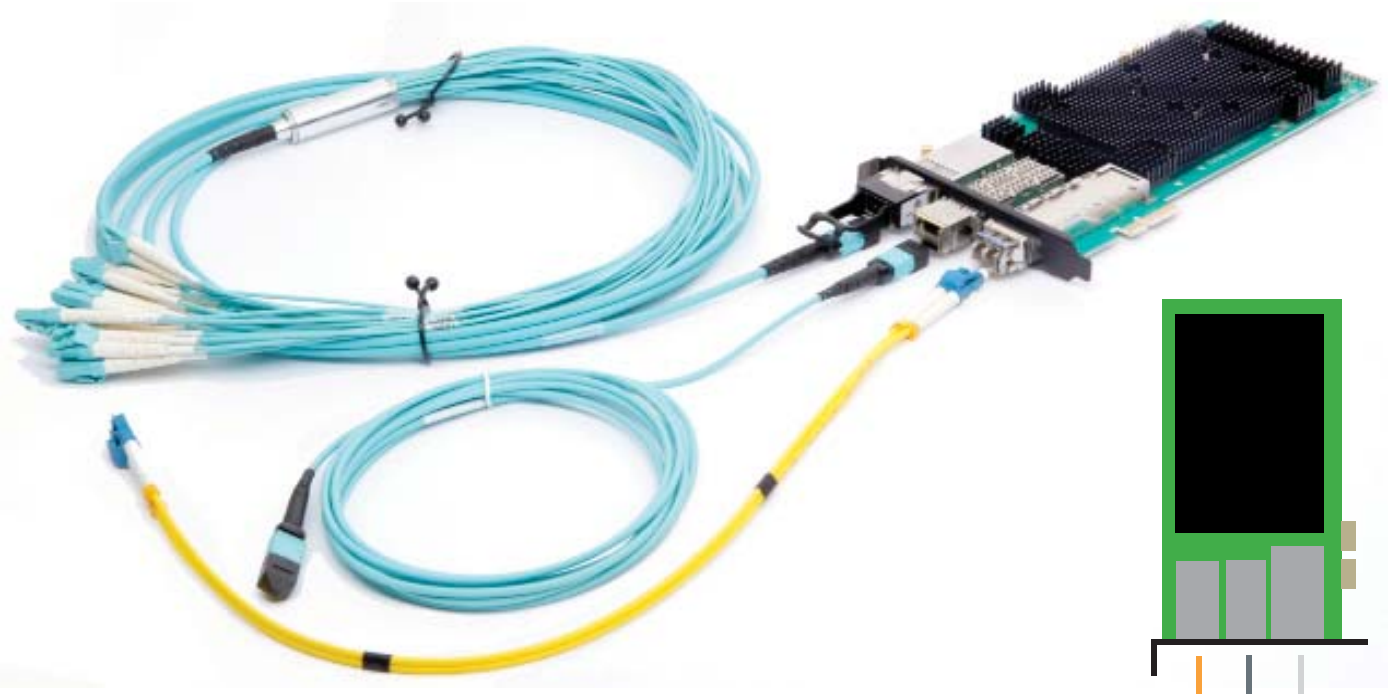
Selectable Tx line rate	Tx line rate can be referenced to either local clock oscillator (adjustable in steps of 1 ppm), SMA input, or from the Rx line rate for Synchronous Ethernet applications. The Tx line rate complies with SONET/SDH/SyncE with respect to wander and jitter.
Jitter attenuation	Selectable loop bandwidth for jitter attenuation: 114 Hz, 229 Hz, 460 Hz, 1864 Hz, or 7834 Hz loop bandwidth
SMA input	• 10.0 MHz, or 2.048 MHz Tx line rate reference clock SMA input (Drift/wander is passed from SMA input to Tx line rate) • 250mV-2.5V, loaded 50 ohm, square wave format

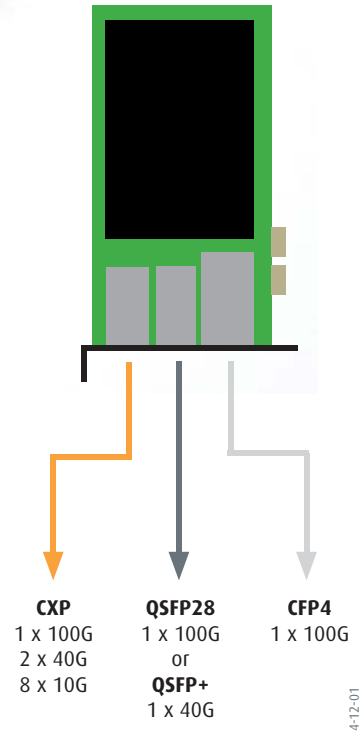
1) Counter size: 64 bits

BETA Version

CAPTURE

Capture criteria	All traffic, stream, FCS errors, filter match, or traffic without test payloads
Capture start/stop triggers	Capture start and stop trigger: none, FCS error, filter match
Capture limit per packet	16 – 9200 bytes
Wire-speed capture buffer per port	256 kB for 100G 128 kB for 40G
Low speed capture buffer per port (10Mbit/s speed)	4096 packets (any size)





The triple media capability of the M1CFP4QSFP28CXP is clearly illustrated here with the trunk cable from the CXP interface ready to provide up to 8 x 10G ports, while the QSFP28 and the CFP4 interfaces each provide a 100G test port.

NOT IN BETA RELEASE:
The following features will first be available in the official release:
- 100GBASE-CR4, 40G BASE-CR4
- 100G FEC
- QSFP+ 40G
- Ethernet Autoneg Control CL72+CL73
- Advanced timing features

SPECIFICATIONS

Dimensions

1U XenaCompact
- W: 19″ (48.26 cm)
- H: 1.75″ (4.45 cm)
- D: 9.8″ (25 cm)
- Weight: 10 lbs (4.5 kg)

4U XenaBay
- W: 19″ (48.26 cm)
- H: 7″ (17.78 cm)
- D: 19.7″ (50 cm)
- Weight: 36.4 lbs (16.5 kg)

Power
- AC Voltage: 100-240V
- Frequency: 50-60Hz
- Max. Power: 90W (XenaCompact) / 120W (XenaBay)
- Max. Current: 0.8A with 120V supply, and 0.4A with 240V supply

Regulatory
- FCC (US), CE (Europe)

Environmental
- Operating Temperature: 10 to 35° C
- Storage Temperature: -40 to 70° C
- Humidity: 8% to 90% non-condensing

Max. Noise
- XenaCompact: 49 dBa
- XenaBay: 58.5 dBa

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