

# Tektronix Logic Analyzers

## TLA6000 Series Data Sheet



### Features & Benefits

- Comprehensive Set of Signal Integrity Tools that Allow You to Quickly Isolate, Identify, and Debug Complex Signal Integrity Issues
  - Glitch Trigger and Storage – Allows you to trigger on and highlight potential signal integrity problems. Not only can the TLA6000 Series trigger on the problem, but by highlighting suspected problems in red, you will be able to easily determine which signals you need to investigate further
  - iCapture – Route the suspected signal to the analog output of the TLA6000 using the exclusive Tektronix iCapture feature. This eliminates the need to double-probe with an oscilloscope probe, reducing time to debug
  - iView – Time-correlated view of both logic analyzer and oscilloscope data to trace the SI problem across the digital and analog domain

- Performance and Ease of Use to Debug, Validate, and Optimize Digital Systems
  - 125 ps Resolution MagniVu™ Acquisition to Accurately See Signal Relationships in Your System
  - State Speed – Sample your fastest synchronous buses with clock rates up to 800 MHz and data rates up to 1.25 Gb/s
  - 15 in. Display, with Optional Touch Screen to See More of Your Data and Navigate Efficiently through Your Data
  - 3 Models with 68/102/136 Channels and Up to 128 Mb Record Length offer Flexible Solutions to Fit Any Budget
  - Drag-and-Drop Triggering – Simply drag any one of eight different trigger types from a table onto the waveform and the TLA will automatically set up the trigger conditions. Eliminates errors, improves repeatability, and saves time
  - Drag-and-Drop Measurements – Simply drag an icon from the measurement toolbar and drop it on your signal of interest and get a table of results. Saves time, removes complexity, and reduces measurement uncertainty
- Analysis Tools for Debugging and Validating Today's Digital Systems
  - FPGA
  - DDR2
  - A Broad Selection of Microprocessor and Bus Support
  - MIPI CSI and DSI Debug

### Applications

- Digital Hardware Validation and Debug
- Monitoring, Measurement, and Optimization of Digital Hardware Performance
- Embedded Software Integration, Debug, and Verification

## Efficiently Debug and Validate Your Digital System at a Price You Will Like!

The affordable TLA6000 Series of logic analyzers offer the performance needed to debug, validate, and optimize the functionality of your digital system. The TLA6000 Series also provides a comprehensive set of signal integrity debug tools that allow you quickly isolate, identify, and characterize elusive and hard-to-find problems. Add a broad range of support for today's applications, and you have the ideal tool to help you meet all of the debug challenges of today's digital designs.

The TLA6000 Series allows you to effectively validate and debug the functionality of your digital designs:

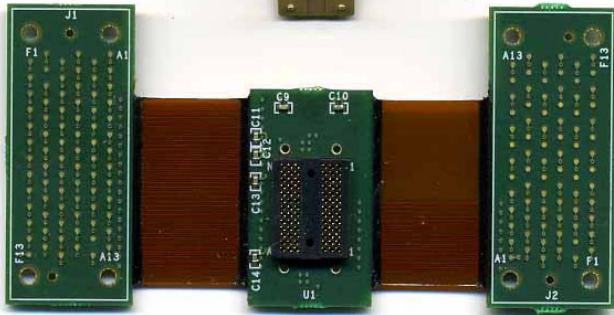
- Use the patented 8 GHz MagniVu technology to accurately measure timing relationships. The single, integrated acquisition architecture of the TLA6000 Series eliminates the timing skew problems inherent in other logic analyzer architectures
- Capture on buses with clock rates up to 800 MHz and data rates up to 1.25 Gb/s
- Buy the capability you need now and upgrade as your measurement needs grow
- Quickly isolate events through a simple and intuitive drag-and-drop trigger setup
- Easily summarize your design's performance with sophisticated drag-and-drop measurements such as frequency, period, pulse width, duty cycle, and edge count
- View data in a variety of time-correlated formats including waveform, listing, graph, disassembly, source code, or compare

## Find Tough Signal Integrity Problems

Today's logic analyzers not only need to help troubleshoot functional issues in your design, but also need to help find signal integrity problems caused by crosstalk, termination mismatches, ground bounce, and other issues. To help debug these problems, the TLA6000 Series includes a comprehensive suite of signal debug tools.

These tools allow you to:

- Use glitch trigger to monitor selected signals in your design and trigger when a signal integrity problem is found on any one of these signals
- Automatically tag any found signal integrity problems, allowing you to quickly identify the signals of interest
- Gain more insight into the problem using the exclusive iCapture functionality to view both digital and analog data through a single probe
- Use iView to see time-correlated digital and analog displays of your data, letting you track the signal integrity problem across both analog and digital domains



Memory Chip Interposer.

## DDR2 Protocol Debug and Validation

DDR2 memory systems are used in many of today's embedded designs – commonly implemented as a bus on the microprocessor or as a block in an FPGA. The complexity of the DDR2 protocol and the number of command/data/address signals make it difficult to both visualize the operation of the bus and to isolate any potential problems. In addition, designers need to ensure that signal timing and interfaces comply with JEDEC standards. The TLA6000 DDR2x8 and DDR2x16 options provide a complete, easy-to-use DDR2 test solution for embedded DDR2 designs up to DDR2-800 using x4, x8, and x16 data-width DDR2 devices.

These options consist of set of tools designed to provide visibility to all address, data, and control signals. The bundle includes:

- Memory chip interposers that provide a convenient way of probing embedded DDR memory systems and eliminates the need to design in probe access points. These memory chip interposers work with the unique iCapture™ Analog Mux feature of the TLA6000 to provide a single probing solution for both the logic analyzer and oscilloscope, saving time and minimizing setup complexity
- Protocol decode software that shows all of the DDR2 transactions as well as providing triggering on DDR2 events
- Sample-point analysis software that automates the process of correctly configuring the TLA6000 Series to accurately sample the DDR2 signals
- Protocol violation software that finds and reports violations of the JEDEC-defined DDR2 protocol

Sample	B_DDR30_2B ADDRESS	B_DDR30_2B WE/WE/WE/CS	B_DDR30_2B DATA1	B_DDR30_2B DATA2
12	-----	DESL - IGNORE COMMAND	-----	-----
13	11DA1	ACT - BANK ACTIVATE (S0W) Bank: 1	-----	-----
14	-----	DESL - IGNORE COMMAND	-----	-----
15	-----	DESL - IGNORE COMMAND	-----	-----
16	-----	DESL - IGNORE COMMAND	-----	-----
17	-----	DESL - IGNORE COMMAND	-----	-----
18	162F8	WB - WRITE (S0W) Bank: 1	-----	-----
19	-----	DESL - IGNORE COMMAND	-----	-----
20	-----	DESL - IGNORE COMMAND	-----	-----
21	-----	DESL - IGNORE COMMAND	-----	-----
22	-----	DESL - IGNORE COMMAND	-----	-----
23	-----	WRITE DATA	00100000	00080000
24	-----	WRITE DATA	00420000	00200000
25	-----	WRITE DATA	01000000	00800000
26	-----	WRITE DATA	04000000	02000000
27	-----	WRITE DATA	10000000	08000000
28	-----	WRITE DATA	40000000	20000000
29	-----	WRITE DATA	00000001	80000000
30	-----	WRITE DATA	00000004	00000002

Protocol Decode Software.

**Protocol Violations**

Sample	Command	Rank	Bank	Row/Col Addr	Error
1633	RD	0	NA	NA	RD command to rank with I/O gating overriding sense a...
1676	RD	0	NA	NA	RD command to rank with I/O gating overriding sense a...
1694	RD	0	NA	NA	RD command to rank with I/O gating overriding sense a...
1712	RD	0	NA	NA	RD command to rank with I/O gating overriding sense a...
1716	RD	0	NA	NA	RD command to rank with I/O gating overriding sense a...
1720	RD	0	NA	NA	RD command to rank with I/O gating overriding sense a...
1724	RD	0	NA	NA	RD command to rank with I/O gating overriding sense a...
1742	RD	0	NA	NA	RD command to rank with I/O gating overriding sense a...
1760	RD	0	NA	NA	RD command to rank with I/O gating overriding sense a...
1778	RD	0	NA	NA	RD command to rank with I/O gating overriding sense a...
1796	RD	0	NA	NA	RD command to rank with I/O gating overriding sense a...

**Error Detail**  
RD command to rank with I/O gating overriding sense amplifiers because of a previous write (WR or WRA) command. Rank requires tNWR(1007tks). Rank received only 392tks.

**Summary**

Name	Value
Total Samples	8194
Total Commands	1557
Errors Found	22
Command Activity	19.00%
Read Activity	11.86%
Write Activity	0.01%
Refresh Commands	2
Precharge Commands	290
Activate Commands	291
MRS Commands	0

**Commands In Time**

Protocol Err: ~1.51 us  
Precharge: ~1.19 ms

Violation Reporting

Utilization Summary of Data

DDR Analysis.

## TLA6000 Selection Guide

Characteristic	TLA6202	TLA6203	TLA6204
Channels	68	102	136
High-speed Timing	8 GHz (125 ps) with 16 Kb record length		
Maximum Timing	2 GHz / 1 GHz / 500 MHz		
Sample Rate (Quarter/Half/Full channel)	450 MHz / 450 MHz / 235 MHz (standard) 625 MHz / 800 MHz / 450 MHz (with Option 45)		
Maximum State Data Rate (Quarter/Half/Full channel)	900 Mb/s / 470 Mb/s / 235 Mb/s (standard) 1.25 Gb/s / 900 Mb/s / 450 Mb/s (with Option 45)		
Maximum Record Length	2 Mb (standard) 8 Mb with Option 1S 32 Mb with Option 2S 128 Mb with Option 3S		
Analog Mux	4 fixed channels (standard) Any signal (user selectable) may be routed to 4 output BNCs with Option AM		
Probing Options	P6810 General-purpose probe with Option 1P – supports single-ended and differential signals Mictor connections with Option 2P P6960 D-Max probe with Option 3P		

## Characteristics

### General

Characteristic	Description
Number of Channels (All channels are acquired including clocks)	
TLA6202	68 channels (4 are clock channels)
TLA6203	102 channels (4 are clock and 2 are qualifier channels)
TLA6204	136 channels (4 are clock and 4 are qualifier channels)
Channel grouping	No limit to number of groups or number of channels per group (all channels can be reused in multiple groups)
Time Stamp	51 bits at 125 ps resolution (3.25 days duration)
Clocking/Acquisition Modes	Asynchronous/Synchronous 8 GHz MagniVu high-speed timing is available simultaneous with all modes
Expansion Capability	The TLA6000 Series can be used as either a master or expansion mainframe in systems consisting of up to 8 TLA6000/TLA7000 instruments. A TL708EX Instrument Hub and Expander is required when connecting 3-8 instruments together using TekLink™ cables

### PC Characteristics

Characteristic	Description
Operating System	Microsoft® Windows® XP Professional and Multilingual User Interface Pack
Processor	2.2 GHz Intel Core 2 Duo T7500
Chipset	Intel® 965GME
Memory	1 GB DDR2 expandable to 2 GB DDR memory
Sound	Line In, Line Out, and Mic Out connectors
Removable Hard Drive	3.5 in., ≥80 GB Serial ATA, 7200 RPM
Optical Drive	Internal 4.7 GB DVD±R/RW
External Display Port Type	One (1) DVI-I (primary – digital and analog) connector and one (1) VGA connector
External Display Resolution	Up to 1600×1200 noninterlaced at 32-bit color, each for both primary and secondary displays
Network Port	Two (2) 10/100/1000 LAN with RJ-45 connector
USB 2.0 Port	Seven (7); three (3) in front and four (4) in rear

### Integral Controls

Characteristic	Description
Front-panel Display	Size: 15 in. (38.1 cm) diagonal Type: Active-matrix color TFT LCD with backlight Resolution: 1024×768
Simultaneous Display Capability	Both the front-panel and one external display can be used simultaneously at 1024×768 resolution
Front Panel	General-purpose knob with dedicated hotkeys and knobs for horizontal and vertical scaling and scrolling
Touch Screen	Available with Option 18

### Integrated View (iView™) Capability

Characteristic	Description
TLA Mainframe Configuration Requirements	<p>GPIO-iView (Opt. 1C) requires TLA Application Software V5.0 or greater</p> <p>USB-iView (Opt. 2C) requires TLA Application Software V5.8 or greater</p>
Number of Tektronix Oscilloscopes that can be Connected to a TLA System	1
External Oscilloscopes Supported	More than 100. For a complete listing of currently supported oscilloscopes, please visit our website <a href="http://www.tektronix.com/iview">http://www.tektronix.com/iview</a>
TLA Connections	USB, Trigger In, Trigger Out, Clock Out
Oscilloscope Connections	
GPIO-iView (Opt. 1C)	GPIO, Trigger In, Trigger Out, Clock In (when available)
USB-iView (Opt. 2C)	USB Device Port, Trigger In, Trigger Out
Setup	iView™ external oscilloscope wizard automates setup
Data Correlation	After oscilloscope acquisition is complete, the data is automatically transferred to the TLA and time correlated with the TLA acquisition data
Deskew	The oscilloscope and TLA data is automatically deskewed and time correlated when using the iView™ external oscilloscope cable
GPIO-iView™ (Opt. 2C) External Oscilloscope Cable Length	2 m (6.6 ft.)
USB-iView (Opt. 2C) External Oscilloscope Cable Length	2 m (6 ft.)

### Symbolic Support

Characteristic	Description
Number of Symbols/Ranges	Unlimited (limited only by amount of virtual memory available on TLA)
Object File Formats Supported	IEEE695, OMF 51, OMF 86, OMF 166, OMF 286, OMF 386, COFF, Elf/Dwarf 1 and 2, Elf/Stabs, TSF (If your software development tools do not generate output in one of the above formats, TSF, or the Tektronix symbol file, a generic ASCII file format is supported. The generic ASCII file format is documented in the TLA User Manual). If a format is not listed, please contact your local Tektronix representative

**External Instrumentation Interfaces**

Characteristic	Description
System Trigger Output	Asserted whenever a system trigger occurs (TTL-compatible output, back-terminated into 50 $\Omega$ )
System Trigger Input	Forces a system trigger (triggers all modules) when asserted (adjustable threshold between 0.5 V and 1.5 V, edge sensitive, falling-edge latched)
External Signal Output	Can be used to drive external circuitry from a module's trigger mechanism (TTL-compatible output, back-terminated into 50 $\Omega$ )
External Signal Input	Can be used to provide an external signal to arm or trigger any or all modules (adjustable threshold between 0.5 V and 1.5 V, level sensitive)

**Power**

Characteristic	Description
Voltage Range/Frequency	90-250 V AC at 45-66 Hz, 100-132 V AC at 360-440 Hz
Input Current	7 A maximum at 90 V AC (70 A surge)
Power Consumption	750 W maximum

**Environmental**

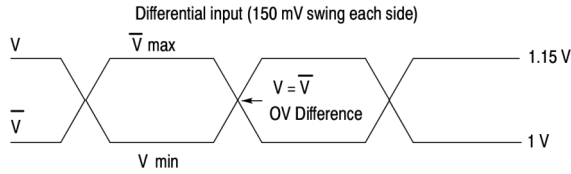
Characteristic	Description
Temperature	Operating: +5 °C to +45 °C Nonoperating: -20 °C to +60 °C
Humidity	20% to 80% Operating: $\leq 30$ °C; 80% relative humidity (29 °C maximum wet-bulb temperature) Nonoperating: 8% to 80% (29 °C maximum wet-bulb temperature)
Altitude	Operating: -1,000 ft. to 10,000 ft. (-305 meters to 3,050 meters)
Safety	UL3111-1, CSA1010.1, EN61010-1, IEC61010-1

**Physical Characteristics**

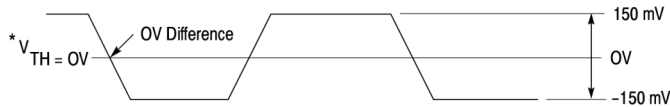
Dimensions	mm	in.
Height	295	11.6
Width	451	17.75
Depth	460	18.1
Weight	kg	lb.
Net	17.1	36.7
Shipping (Typical)	30.1	66.7

**Input Characteristics (with P6800 or P6900 Series probes)**

Characteristic	Description
Capacitive Loading	0.5 pF clock/data (P6900 Series) <0.7 pF clock/data (P6800 Series) (1.0 pF for P6810 in group configuration)
Threshold Selection Range	From -2.0 V to +4.5 V in 5 mV increments Threshold presets include TTL (1.5 V), CMOS (1.65 V), ECL (-1.3 V), PECL (3.7 V), LVPECL (2.0 V), LVCMOS 1.5 V (0.75 V), LVCMOS 1.8 V (0.9 V), LVCMOS 2.5 V (1.25 V), LVCMOS 3.3 V (1.65 V), LVDS (0 V), and user defined
Threshold Selection Channel Granularity	Separate selection for each of the clock/qualifier channels and one per group of 16 data channels for each 34-channel probe
Threshold Accuracy (including probe)	$\pm(35 \text{ mV} + 1\%)$
Input Voltage Range	
Operating	-2.5 V to 5.0 V
Nondestructive	$\pm 15$ V
Minimum Input Signal Swing	300 mV (single ended) $V_{\text{MAX}} - V_{\text{MIN}} > 150$ mV (differential)
Input Signal Minimum Slew Rate	200 mV/ns typical



Differential equivalent signal input (300 mV swing) as viewed by the logic analyzer and the analog probe output\*\*.



\* Note: For differential inputs, the module threshold should be set to OV (assuming no common mode error).

\*\* Note: See online help for further analog output details.

**State Acquisition Characteristics  
(with P6800 or P6900 Series probes)**

Full Channel	Half Channel	Quarter Channel
235 MHz	450 MHz / 450 Mb/s or 470 Mb/s (DDR)	450 MHz / 900 Mb/s
450 MHz Optional	800 MHz / 800 Mb/s or 900 Mb/s (DDR)	625 MHz / 1.25 Gb/s

Note: When using SQUIRE adapters, the maximum clock rate / data rate is 300 MHz / 600 Mb/s.

Characteristic	Description
State Record Length with Time Stamps	(Quarter/Half/Full channels) 8/4/2 Mb, 32/16/8 Mb, 128/64/32 Mb, 512/256/128 Mb per channel
Setup-and-Hold Time Selection Range	From 16 ns before, to 8 ns after clock edge in 125 ps increments. Range may be shifted towards the setup region by 0 ns [+8, -8] ns, 4 ns [+12, -4] ns, or 8 ns [+16, 0] ns
Setup-and-Hold Window	
All channels	625 ps typical
Single channel	500 ps typical
Minimum Clock Pulse Width	500 ps, 700 ps (P6810)
Active Clock Edge Separation	400 ps
Demux Channel Selection	Channels can be demultiplexed to other channels through user interface with 8-channel granularity

**Timing Acquisition Characteristics  
(with P6800 or P6900 Series probes)**

Characteristic	Description
MagniVu™ Timing	125 ps max, adjustments to 250 ps, 500 ps, 1 ns, and 2 ns
MagniVu Timing Record Length	16 Kb per channel, with adjustable trigger position
Deep Timing Resolution (Quarter/Half/Full channels)	500 ps / 1 ns / 2 ns to 50 ms
Deep Timing Resolution with Glitch Storage Enabled	4 ns to 50 ms
Deep Timing Record Length (Quarter/Half/Full channels with time stamps and with or without transitional storage)	8/4/2 Mb, 32/16/8 Mb, 128/64/32 Mb, 512/256/128 Mb per channel
Deep Timing Record Length with Glitch Storage Enabled	Half of default main memory depth
Channel-to-Channel Skew	300 ps typical
Minimum Recognizable Pulse/Glitch Width (Single channel)	500 ps (P6960, P6964, P6980, P6982, P6860, P6864, P6880), 750 ps (P6810)
Minimum Detectable Setup/Hold Violation	250 ps
Minimum Recognizable Multichannel Trigger Event	Sample period + channel-to-channel skew

**Analog Acquisition Characteristics  
(with P6800 or P6900 Series probes)**

Characteristic	Description
Bandwidth	2 GHz typical
Attenuation	10X, ±1%
Offset and Gain (Accuracy)	±50 mV, ±2% of signal amplitude
Channels Demultiplexed	4
Run/Stop Requirements	None, analog outputs are always active
iCapture™ Analog Outputs	Compatible with any supported Tektronix oscilloscope
iCapture Analog Output BNC Cable	Low loss, 10X, 36 in. Basic Analog Multiplexer functionality is offered standard on all TLA6000 models. This routes 4 fixed channels to the iCapture Analog Output BNCs. The outputs cannot be switched to other logic analyzer channels. Option AM enables full analog multiplexer control and allows the routing of any 4 logic analyzer channels to the iCapture Analog Output BNCs

**Trigger Characteristics**

Characteristic	Description
Independent Trigger States	16
Maximum Independent If/Then Clauses per State	16
Maximum Number of Events per If/Then Clause	8
Maximum Number of Actions per If/Then Clause	8
Maximum Number of Trigger Events	18 (2 counters/timers plus any 16 other resources)
Number of Word Recognizers	16
Number of Transition Recognizers	16
Number of Range Recognizers	4
Number of Counters/Timers	2
Trigger Event Types	Word, Group, Channel, Transition, Range, Anything, Counter Value, Timer Value, Signal, Glitch, Setup-and-Hold Violation, Snapshot
Trigger Action Types	Trigger Module, Trigger All Modules, Trigger Main, Trigger MagniVu, Store, Don't Store, Store Sample, Increment Counter, Decrement Counter, Reset Counter, Start Timer, Stop Timer, Reset Timer, Snapshot Current Sample, Goto State, Set/Clear Signal, Do Nothing
Maximum Triggerable Data Rate	1250 Mb/s (4X clocking mode)
Trigger Sequence Rate	DC to 500 MHz (2 ns)
Counter/Timer Range	51 bits each (>50 days at 2 ns)
Counter Rate	DC to 500 MHz (2 ns)
Timer Clock Rate	500 MHz (2 ns)
Counter/Timer Latency	2 ns
Range Recognizers	Double bounded (408 channel max). Can be as wide as any group, must be grouped according to specified order of significance
Setup-and-Hold Violation Recognizer Setup Time Range	From 8 ns before to 7 ns after clock edge in 125 ps increments. This range may be shifted towards the positive region by 0 ns, 4 ns, or 8 ns
Setup-and-Hold Violation Recognizer Hold Time Range	From 7 ns before to 8 ns after clock edge in 125 ps increments. This range may be shifted towards the positive region by 0 ns [+8, -8] ns, 4 ns [+12, -4] ns, or 8 ns [+16, 0] ns
Trigger Position	Any data sample
MagniVu Trigger Position	MagniVu position can be set from 0% to 60% centered around the MagniVu trigger
Storage Control (Data qualification)	Global (conditional), by state (start/stop), block, by trigger action, or transitional. Also force main prefill selection available

**Ordering Information****TLA6202**

68-channel Logic Analyzer module, 8 GHz timing, 235 MHz state, 2 Mb record length. Options for up to 128 Mb record length and/or up to 450 MHz state.

**TLA6203**

102-channel Logic Analyzer module, 8 GHz timing, 235 MHz state, 2 Mb record length. Options for up to 128 Mb record length and/or up to 450 MHz state.

**TLA6204**

136-channel Logic Analyzer module, 8 GHz timing, 235 MHz state, 2 Mb record length. Options for up to 128 Mb record length and/or up to 450 MHz state.

**All Include:** Mini Keyboard (119-7275-xx), Optical Wheel Mouse (119-7054-xx), Front-panel cover (200-4939-xx), TLA Application Software CD (063-3881-xx), Certificate of Traceable Calibration.

**Note:** Please specify probe, power, language, and service options when ordering.

**Instrument Options**

Option	Description
1P	Add full complement of P6810 (General-purpose) probes
2P	Add full complement of P6434 (Mictor) probes. Includes SQUIRE adapters
3P	Add full complement of P6960 (D-Max) probes
1S	Increase to 8 Mb record length
2S	Increase to 32 Mb record length
3S	Increase to 128 Mb record length
DDR2x8	DDR2 Analysis for x4 and x8 Devices; includes Socketed Memory Chip Interposer and necessary cables (TLA6203 and TLA6204 only) (requires TLA Application SW V5.8 or greater)
DDR2x16	DDR2 Analysis for x16 Devices; includes Socketed Memory Chip Interposer and necessary cables (TLA6204 only) (requires TLA Application SW V5.8 or greater)
45	Increase state speed to 450 MHz
AM	Add full analog mux control
18	Add touch screen
1C	Add GPIB-iView™ external oscilloscope cable kit (requires TLA Application SW V5.0 or greater)
2C	Add USB-iView external oscilloscope cable kit (requires TLA Application SW V5.8 or greater)
PO	Add accessory pouch
TL	Add TekLink cable

**Recommended Accessories**

Accessory	Description
Logic Analyzer Cart	
LACART	2-shelf Cart
K4000	3-shelf Cart
016-1522-xx	Wheeled Transport Case
020-2664-xx	Rackmount Kit
650-4815-xx	Additional Removable Hard Drive Assembly; No SW

**Power Plug Options**

Option	Description
A0	North America power
A1	Universal Euro power
A2	United Kingdom power
A3	Australia power
A4	240 V, North America power
A5	Switzerland power
A6	Japan power
A10	China power
A11	India power
A12	Brazil power
A99	No power cord or AC adapter

**Language Options**

Option	Description
L0	English Manual
L5	Japanese Manual
L10	Russian Manual
L99	No Manual

**Service Options**

Option	Description
C3	Calibration Service 3 Years
C5	Calibration Service 5 Years
D1	Calibration Data Report
D3	Calibration Data Report 3 Years (with Option C3)
D5	Calibration Data Report 5 Years (with Option C5)
R3	Repair Service 3 Years
R5	Repair Service 5 Years
S1	On-site Service 1 Year
S3	On-site Service 3 Years (with R or C options)
R3DW	Repair Service Coverage 3 Years (includes product warranty period). 3-year period starts at time of instrument purchase
R5DW	Repair Service Coverage 5 Years (includes product warranty period). 5-year period starts at time of instrument purchase

**Upgrades**

You can increase the state speed, memory depth, or add full analog multiplexer capability to existing TLA6000 models by ordering the appropriate upgrade kit. Please refer to the TLA Family Upgrade Guide for further details.



Tektronix is registered to ISO 9001 and ISO 14001 by SRI Quality System Registrar.



Product(s) complies with IEEE Standard 488.1-1987, RS-232-C, and with Tektronix Standard Codes and Formats.









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\* European toll-free number. If not accessible, call: +41 52 675 3777

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