



# Xena M2QSFP+

The M2QSFP+ is a 2-port 40GBASE Quad Small Form-Factor Pluggable Plus (QSFP+) test module for our XenaCompact and XenaBay chassis. This dual-speed test module provides 2 x 40G or 8 x 10G test ports via a simple software configuration and is compatible with 40G QSFP+ compliant transceiver modules, using MPO connectors. It delivers a breakthrough price/performance benchmark for PRBS, load-stress, and functional testing of Ethernet equipment and network infrastructure.



40/10G	XenaCompact: XenaBay:	<b>C1-M2QSFP+</b> <b>M2QSFP+</b>
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### TOP FEATURES

- Supports QSFP+
- Price/performance
- Dual-speed (40G /10G) testing
- Free software (incl. XenaManager-2G, XenaIntegrator, XenaScripting, Xena2544, Xena1564, Xena3918, and Xena2889)
- Free 12-month hardware warranty
- 36 months free software updates
- Free tech support product lifetime

## PORT LEVEL FEATURES

Interface category	40G and 10G Ethernet
Number of test ports	2 x 40G / 8 x 10G (software configurable)
Interface options	<ul style="list-style-type: none"> <li>• 2 x 40GBASE-LR4</li> <li>• 2 x 40GBASE-SR4</li> <li>• 2 X 40G Copper Direct Attached Cable (QSFP+)<sup>1)</sup></li> <li>• 8 x 10GBASE-ISR4/ISM4 (QSFP+ to 4 x 10GE breakout)<sup>2)</sup></li> <li>• 8 x 10G Copper Direct Attached Cable (QSFP+ to 4 x 10GE SFP+ breakout)</li> </ul>
Number of transceiver module cages	2 x QSFP+
Port statistics <sup>2)</sup>	Link state, FCS errors, pause frames, ARP/PING, error injections, training packet All traffic: RX and TX Mbit/s, packets/s, packets, bytes Traffic w/o test payload: RX and TX Mbit/s, packets/s, packets, bytes
Adjustable Inter Frame Gap (IFG)	Configurable from 16 to 56 bytes, default is 20B (12B IFG + 8B preamble)
Transmit line rate adjustment	Ability to adjust effective line rate by forcing idle gaps equivalent to -1000 ppm (increments of 10 ppm)
Transmit line clock adjustment	From -400 to 400 ppm in steps of 0.001 ppm (shared across all ports)
ARP/PING	Supported (configurable IP and MAC address per port)
Field upgradeable	System is fully field upgradeable to product releases (FPGA images and Software)
Tx disable	Enable/disable of optical laser or copper link
IGMPv2 multicast join/leave	IGMPv2 continuous multicast join, with configurable repeat interval
Histogram statistics <sup>3)</sup>	Two real-time histograms per port. Each histogram can measure one of RX/TX packet length, IFG, or Latency distribution for all traffic, a specific stream, or a filter
Loopback modes	<ul style="list-style-type: none"> <li>• L1RX2TX – RX-to-TX, transmit byte-by-byte copy of the incoming packet</li> <li>• L2RX2TX – RX-to-TX, swap source and destination MAC addresses (<i>*only at 10G</i>)</li> <li>• L3RX2TX – RX-to-TX, swap source and destination MAC addresses and IP addresses (<i>*only at 10G</i>)</li> <li>• TXON2RX – TX-to-RX, packet is also transmitted from the port</li> <li>• TXOFF2RX – TX-to-RX, port's transmitter is idle</li> <li>• Port-to-port – Inline loop mode where all traffic is looped 100% transparent at L1</li> </ul>
Oscillator characteristics	<ul style="list-style-type: none"> <li>• Initial Accuracy is 3 ppm</li> <li>• Frequency drift over 1st year: +/- 3 ppm (over 15 years: +/- 15 ppm)</li> <li>• Temperature Stability: +/- 20 ppm (Total Stability is +/- 35 ppm)</li> </ul>

## 40G PRBS AND PCS LAYERS

Payload Test pattern	PRBS 2 <sup>31</sup> -1
Error Injection	Manual single shot bit-errors or bursts, automatic continuous error injection
Frame size and header	Fixed size from 56 to 9200 bytes, any layer 2/3/4 frame header
Alarms	Pattern loss, bit-error rate threshold
Error analysis	bit-errors: seconds, count, rate mismatch '0' / '1': seconds, count, rate logging and analysis of bit-error event timing
PCS virtual lane configuration	User-defined skew insertion per Tx virtual lane, and user defined virtual lane to SerDes mapping for testing of the Rx PCS virtual lane re-order function.
PCS virtual lane statistics	Relative virtual lane skew measurement (up to 2048 bits), sync header and PCS lane marker error counters, indicators for loss of sync header and lane marker, BIP8 errors



### TRANSMIT ENGINES

Number of transmit streams per port	64 (wire-speed)
	Each stream can generate millions of traffic flows through the use of field modifiers
Test payload insertion per stream	Wire-speed packet generation with timestamps, sequence numbers, and data integrity signature optionally inserted into each packet.
Stream statistics <sup>2)</sup>	TX Mbit/s, packets/s, packets, bytes, FCS error, Pause
Bandwidth profiles	Burst size and density can be specified. Uniform and bursty bandwidth profile streams can be interleaved.
Field modifiers	16-bit header field modifiers with inc, dec, or random mode. Each modifier has configurable bit-mask, repetition, min, max, and step parameters. 2 modifiers per stream
Packet length controls	Fixed, random, butterfly, and incrementing packet length distributions (from 56 to 9200 bytes)
Packet payloads	Repeated user specified 1 to 18B pattern, a 8-bit incrementing pattern
Error generation	Undersize length (56B min) and oversize length (9200 max.) packet lengths, injection of sequence, disorder, payload integrity, and FCS errors
TX packet header support and RX autodecodes	Ethernet, Ethernet II, VLAN, ARP, IPv4, IPv6, UDP, TCP, LLC, SNAP, GTP, ICMP, RTP, RTCP, STP, MPLS, PBB, or fully specified by user
Packet scheduling modes	<ul style="list-style-type: none"> <li>• Normal (stream interleaved mode). Standard scheduling mode, precise rates, minor variation in packet inter-frame gap.</li> <li>• Strict Uniform. New scheduling mode, with 100% uniform packet inter-frame gap, minor deviation from configured rates</li> <li>• Sequential packet scheduling (sequential stream scheduling). Streams are scheduled continuously in sequential order, with configurable number of packets per stream</li> </ul>

### RECEIVE ENGINE

Number of traceable Rx streams per port	512 (wire-speed)
Automatic detection of test payload for received packets	Real-time reporting of statistics and latency, loss, payload integrity, sequence error, and disorder error checking
Jitter measurement	Jitter (Packet Delay Variation) measurements compliant to MEF10 standard with 8 ns accuracy
Stream statistics <sup>3)</sup>	<ul style="list-style-type: none"> <li>• RX Mbit/s, packets/s, packets, bytes.</li> <li>• Loss, payload integrity errors, sequence errors, disorder errors</li> <li>• Min latency, max latency, average latency</li> <li>• Min jitter, max jitter, average jitter</li> </ul>
Latency measurements accuracy	±16 ns
Latency measurement resolution	8 ns ( <i>Latency measurements can calibrate and remove latency from transceiver modules</i> )
Number of filters:	<ul style="list-style-type: none"> <li>• 4 x 64-bit user-definable match-term patterns with mask, and offset</li> <li>• 4 x frame length comparator terms (longer, shorter)</li> <li>• 4 x user-defined filters expressed from AND/OR'ing of the match and length terms.</li> </ul>
Filter statistics <sup>3)</sup>	Per filter: RX Mbit/s, packets/s, packets, bytes.

### CAPTURE

Capture criteria	All traffic, stream, FCS errors, filter match, or traffic without test payloads
Capture start/stop triggers	Capture start and stop trigger: none, FCS error, filter match
Capture limit per packet	16 – 9200 bytes
Wire-speed capture buffer per port	128 kB
Low speed capture buffer per port (10Mbit/s speed)	4096 packets (any size)

1) The interface implements discrete PHY devices with built-in EDC support that employs sophisticated signal processing techniques to recover a 10 Gbps signal that has travelled over a dispersive copper Direct Attach Cable (DAC) and restore a bit-error rate of 10-12 or better. 40GBASE-CR4 Auto-Negotiation is **not** supported.

2) **ISR4** - where "i" represents interoperability between the QSFP+ transceiver with any 10GBASE-SR compliant modules. For **ISM4**, the "i" represents interoperability between the QSFP+ transceiver with any single mode (SM) 10GBASE-LR compliant modules up to 2 km link length.

3) Counter size: 64 bits

### SPECIFICATIONS

#### Dimensions

##### 1U XenaCompact

- W: 19" (48.26 cm)
- H: 1.75" (4.45 cm)
- D: 9.8" (25 cm)
- Weight: 10 lbs (4.5 kg)

##### 4U XenaBay

- W: 19" (48.26 cm)
- H: 7" (17.78 cm)
- D: 19.7" (50 cm)
- Weight: 36.4 lbs (16.5 kg)
- Slots: 1 slot in XenaBay

#### Power

- AC Voltage: 100-240V
- Frequency: 50-60Hz
- Max. Power: 90W (XenaCompact) / 120W (XenaBay)
- Max. Current: 0.8A with 120V supply, and 0.4A with 240V supply

#### Regulatory

- FCC (US), CE (Europe)

#### Environmental

- Operating Temperature: 10 to 35° C
- Storage Temperature: -40 to 70° C
- Humidity: 8% to 90% non-condensing

#### Max. Noise

- XenaCompact: 49 dBA
- XenaBay: 58.5 dBA



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