Product Order Number

10G & 1G	XenaCompact:	**C1-M2SFP+4SFP**

M2SFP+4SFP

2-port 10G and 4-port 1G L2-3 test module

The M2SFP+4SFP is a wire-speed 2-port 10GigE and 4-port 1GigE test module. Based on Xena's advanced architecture, the M2SFP+4SFP is a highly flexible and cost-effective solution for testing both 10G and 1G Ethernet at Layers 2-3. Available only in our 1U XenaCompact chassis, this is a robust and easy-to-transport solution.

The M2SFP+4SFP comes complete with Xena's free XenaManager-2G software - an easy-to-use GUI for handling both routine and advanced test schedules that includes XenaScripting, XenaIntegrator, Xena2544, Xena1564, Xena3918 and Xena2889.

TOP FEATURES - M2SFP+4SFP

- Flexibility
- Price/performance
- Ease of use
- Advanced architecture
- Browser-based access via XenaWeb
- Free software (incl. XenaManager-2G, XenaScripting, XenaIntegrator, Xena2544, Xena1564, Xena3918 and Xena2889)
- Free software updates (3 years)
- Free hardware warranty (1 year)
- Free tech support (product lifetime)

Test both 10G and 1G Ethernet from the same robust 1U test chassis

PORT LEVEL FEATURES

Interface categories	10G and 1G Ethernet
Number of test ports	2 x 10G and 4 x 1G
Interface options	2 x 10GBASE-SR / LR / ER / Direct Attached Cable (DAC) [1] and 4 x 10/100/1000BASE-T [2] or 1000BASE-X (SFP-MSA) or 100BASE-FX [3] or 100BASE-BX [3]
Number of transceiver module cages	2 x SFP+ and 4 x SFP
Port statistics [4]	Link state, FCS errors, pause frames, ARP/PING, error injections, training packet All traffic: RX and TX Mbit/s, packets/s, packets, bytes Traffic w/o test payload: RX and TX Mbit/s, packets/s, packets, bytes
Adjustable Inter Frame Gap (IFG)	Configurable from 16 to 56 bytes, default is 20B (12B IFG + 8B preamble)
Transmit line rate adjustment	Ability to adjust the effective line rate by forcing idle gaps equivalent to -1000 ppm (increments of 10 ppm)
Transmit line clock adjustment	From -400 to 400 ppm in steps of 0.001 ppm (shared across all ports)
ARP/PING	Supported (configurable IP and MAC address per port)
Field upgradeable	System is fully field upgradeable to product releases (FPGA images and Software)
Histogram statistics [4]	Two real-time histograms per port. Each histogram can measure one of RX/TX packet length, IFG, or latency distribution for all traffic, a specific stream, or a filter
Tx disable	Enable/disable of optical laser or copper link
IGMPv2 multicast join/leave	IGMPv2 continuous multicast join, with confi gurable repeat interval
Loopback modes	• L1RX2TX – RX-to-TX, transmit byte-by-byte copy of the incoming packet • L2RX2TX – RX-to-TX, swap source and destination MAC addresses • L3RX2TX – RX-to-TX, swap source and destination MAC addresses and IP addresses • TXON2RX – TX-to-RX, packet is also transmitted from the port • TXOFF2RX – TX-to-RX, port's transmitter is idle • Port-to-port – Inline loop mode where all traffic is looped 100% transparent at L1
Oscillator characteristics	• Initial Accuracy is 3 ppm • Frequency drift over 1st year: +/- 3 ppm (over 15 years: +/- 15 ppm) • Temperature Stability: +/- 20 ppm (Total Stability is +/- 35 ppm)

TRANSMIT ENGINE

Number of transmit streams per port	32 (wire-speed) for 1G ports and 256 (wire-speed) for 10G ports. Each stream can generate millions of traffic flows through the use of field modifiers
Test payload insertion per stream	Wire-speed packet generation with timestamps, sequence numbers, and data integrity signature optionally inserted into each packet.
Stream statistics [4]	TX Mbit/s, packets/s, packets, bytes, FCS error, Pause
Bandwidth profiles	Burst size and density can be specified. Uniform and bursty bandwidth profile streams can be interleaved
Field modifiers	16-bit header field modifiers with inc, dec, or random mode. Each modifier has configurable bit-mask, repetition, min, max, and step parameters. 2 modifiers per stream for 1G ports and 5 modifiers per stream for 10G ports.
Packet length controls	Fixed, random, butterfly, and incrementing packet length distributions. Packet length from 56 to 16384 bytes
Packet payloads	Repeated user specified 1 to 18B pattern, a 8-bit incrementing pattern
Error generation	Undersize length (56B min) and oversize length (16384 max.) packet lengths, injection of sequence, misorder, payload integrity, and FCS errors
TX packet header support and RX autodecodes	Ethernet, Ethernet II, VLAN, ARP, IPv4, IPv6, UDP, TCP, LLC, SNAP, GTP, ICMP, RTP, RTCP, STP, MPLS, PBB, or fully specified by user
Packet scheduling modes	• Normal (stream interleaved mode). Standard scheduling mode, precise rates, minor variation in packet inter-frame gap. • Strict Uniform. New scheduling mode, with 100% uniform packet inter-frame gap, minor deviation from configured rates • Sequential packet scheduling (sequential stream scheduling). Streams are scheduled continuously in sequential order, with configurable number of packets per stream

RECEIVE ENGINE

Number of traceable Rx streams per port	680 (wire-speed) for 1G ports and 2048 (wire-speed) for 10G ports
Automatic detection of test payload for received packets	Real-time reporting of statistics and latency, loss, payload integrity, sequence error, and misorder error checking
Jitter measurement	Jitter (Packet Delay Variation) measurements compliant to MEF10 standard with 8 ns accuracy
Stream statistics [4]	• RX Mbit/s, packets/s, packets, bytes. • Loss, payload integrity errors, sequence errors, misorder errors • Min latency, max latency, average latency • Min jitter, max jitter, average jitter
Latency measurements accuracy	±16/32 ns (opto/elec) for 1G ports and ±8 ns for 10G ports
Latency measurement resolution	8 ns *(Latency measurements can calibrate and remove latency from transceiver modules)*
Number of filters:	6 x 64-bit user-definable match-term patterns with mask, and offset 6 x frame length comparator terms (longer, shorter) 6 x user-defined filters expressed from AND/OR'ing of the match and length terms.
Filter statistics [4]	Per filter: RX Mbit/s, packets/s, packets, bytes.

CAPTURE

Capture criteria	All traffic, stream, FCS errors, filter match, or traffic without test payloads
Capture start/stop triggers	Capture start and stop trigger: none, FCS error, filter match
Capture limit per packet	16 – 16384 bytes
Wire-speed capture buffer per port	16 kB for 1G ports and 64 kB for 10G ports
Low speed capture buffer per port (10Mbit/sec)	4096 packets (any size)

1. *The interface implements discrete PHY devices with built in EDC support that employs sophisticated signal processing techniques to recover a 10 Gbps signal that has travelled over a dispersive Copper Direct attach cable and restore a bit-error rate of 10-12 or better.*
2. *Requires Finisar SFP transceivers FCLF-8521-3 with sgmii host interface*
3. *Requires Source Photonics SFP transceivers with sgmii host interface*
4. *Counter size: 64 bits*

SPECIFICATIONS

Dimensions

1U XenaCompact
- W: 19″ (48.26 cm)
- H: 1.75″ (4.45 cm)
- D: 9.8″ (25 cm)
- Weight: 10 lbs (4.5 kg)

4U XenaBay
- W: 19″ (48.26 cm)
- H: 7″ (17.78 cm)
- D: 19.7″ (50 cm)
- Weight: 36.4 lbs (16.5 kg)

Power
- AC Voltage: 100-240V
- Frequency: 50-60Hz
- Max. Power: 90W (XenaCompact) / 120W (XenaBay)
- Max. Current: 0.8A with 120V supply, and 0.4A with 240V supply

Regulatory
- FCC (US), CE (Europe)

Environmental
- Operating Temperature: 10 to 35° C
- Storage Temperature: -40 to 70° C
- Humidity: 8% to 90% non-condensing

Max. Noise
- XenaCompact: 49 dBa
- XenaBay: 58.5 dBa

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