JDSU ONT-503/506/512 Optical Network Tester

100G Test Solution supporting 40GE/100GE/OTU4 – Preliminary

Key features

- Powerful test solution designed to address the 40GE, 100GE and OTU4 test and development needs of key component makers, transponder and system manufacturers

- Testing and validation of electrical and optical level functionality with unframed BERT, PCS Layer (formerly MLD), Ethernet and IP traffic

- Ready for both 40GE and100GE. OTU4 traffic support when standards clearly defined

- The transponder carry card concept allows the ONT solution to support current and future types of 40GE/100GE/OTU4 transponders

- Applications aligned to needs and timing of market – in depth hardware and physical layer applications followed by comprehensive applications for Ethernet, IP and OTU4

Overview

40GE, 100GE and OTU4 are here and the challenge of transition from a proof of concept into an economically viable product must be met. The technical discontinuities driven by 40GE and 100GE are formidable and without the correct test and measurement equipment they are nearly impossible. The 100G test solution is specifically designed from the ground up to meet the needs of developers, manufacturers and installers of 40GE,100GE and OTU4 equipment. It offers full scalability to cover the current and future challenges of hardware, firmware and software development through manufacturing and installation and into the turn up phase.

Target Applications

- Component manufacturers through the powerful and flexible electrical interface (via an adapter) and unframed BERT stream generation and lambda mapping with migration up to L3 and beyond
- Transponder manufacturers who need to develop and then validate at both the electrical and optical interfaces to ensure full compatibility and interoperability
- System manufacturers who need to integrate complex 40GE, 100GE and OTU4 elements into equipment. Validation and verific tion of key components against standards
- Service providers who want to adopt and install 40GE, 100GE and OTU4 equipment at critical aggregation points and ensure full and seamless validation and verification of interoperability with current equipment and OTU4

Technical Description
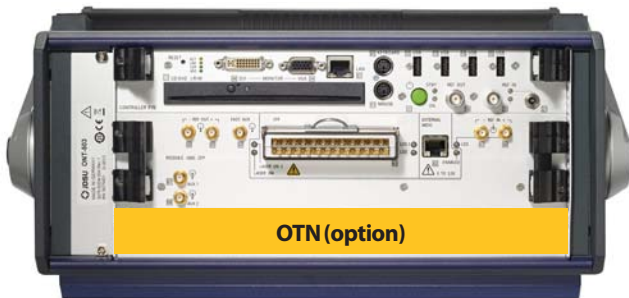
100G test solution in a portable unit
Ideal for turn-up phase!

Above: The 100G test solution fit ed to our ONT-503 mainframe

Transponder Carry Card

At the heart of the power and flexibility of the 100G test solution is the concept of our transponder carrier card. The board allows the critical high speed differential electrical signals from our 100G BERT engine to be interfaced with transponders, ICs, systems or any other 100G element that needs to be developed, tested, manufactured and commissioned.

Via a high speed interface we bring the CAUI/XLAUI signals through retiming and hand the signals off to the interface under test. Initially this will be CFP but later interfaces include CXP and QSFP as well as versions for transport based on the proposed OIF MSA for 100G DWDM transponders. Electrical access is delivered by a CFP to CFP adapter cable which simply plugs into the CFP slot and allows the 100G electrical signals to be delivered to units or components under test.

100G BERT Engine

The 100G BERT Engine handles all the Ethernet (L3 and below) requirements and contains a powerful array of BERTs, framers and MACs. It also contains low noise synthesizers developed from our market leading jitter solutions to allow precise control of the clocks across the full range required. High speed capture memory allows capture of packets and even low level raw data to help debug difficult hardware challenges. The engine is ready for 40GE, 100GE and OTU4 applications and builds on our leadership in high bit rate transport and datacom test and measurement.

Interfaces and I/O

One transponder carry card must be fitted on the 100G test solution[1]

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1 Initially CFP will be offered with CXP likely to follow shortly. Other interfaces will depend on timing and market needs.

TX and RX clocks have a nominal rate of 10.3125 GHz per lane but this will be extended to faster rates as the technology allows (i.e. 11.18G for OTU4 applications). TX clock rate is adjustable in 0.1 ppm increments to ± 500 ppm (note: the actual transponder used may set a lower range).

TX clock can be driven by internal reference, recovered from RX or locked to external clock reference (via standard ONT mainframe synchronization inputs or via High Speed Sync Clock input below).

CFP interface

- In accordance with the CFP MSA Draft 1.0
- Reference clock 1/16 and 1/64 of electrical lane rate switchable
- Power class 1, 2 and 3. Class 4 depending on transponder actual power consumption
- External MDIO access

External I/O

- **Fast trigger output (50 ohm single ended on SMA)**
  - General purpose high speed, low jitter output
  - Nominally 400 mV into 50 ohms
  - Initially supports fast clock output (1/4 lane clock rate). Planned applications include TX pattern trigger and RX trigger on bit error.
    TX pattern trigger allows triggering on a set point in the transmit pattern. Via the RX board capturing a bit error, the trigger can be adjusted to give a trigger when a bit error occurs. This allows the operator to examine the signal leading to the bit errors
- **Two general purpose I/O triggers (SMA)**
  - These are two general purpose I/Os with application specific functions (TBD)
- **TX clock output (differential on 2 x SMA)**
  - Nominally 800 mV into 100 ohms differential
  - A clock signal at a sub-multiple of the transmitter clock – 1/16 or 1/64 of the electrical lane rate selectable (i.e. 1/16 = 644.53 MHz for 40GE and 100GE applications). This can be used for synchronization purposes or to trigger for eye diagrams
- **High-speed sync clock input (differential on 2 x SMA)**
  - Range of 100 mV to 1000 mV into 100 ohms differential
  - Pull in range of > 100 ppm
  - Input clock reference to allow TX clock to be frequency locked to an external clock at a 1/16 of the nominal electrical lane rate
    - 644.53 MHz for 40GE and 100GE
    - 672.16 MHz for OTU3
    - 698.81 MHz for OTU4
  - Indicator LED for signal present
  - GUI indicates signal in lock with internal PLLs

- **External access to transponder serial control (MDIO) bus**
  - The transponder is normally controlled by the ONT application software but the ability exists to directly control the MDIO bus externally for applications such as transponder fi mware development. A front panel connector allows external MDIO access. The MDIO bus is brought out via a RJ45 connector – pin-out is available on request

LEDs on the front panel indicate transponder laser on and transponder indicated loss of signal (LOS). Another LED indicates the presence of the sync clock input .

Applications and Measurement Capability

1st release – key feature overview (over native electrical or CFP interface)

Unframed 10 channel BERT

Data rates supported (per signal channel)

- 10.3125 Gb/s = 40GE and 100GE
- 10.764 Gb/s = OTU3
- 11.18 Gb/s = OTU4

TX

- 32 bit data word, square wave, 2^9, 2^{23} and 2^{31} PRBS test patterns
- Each channel clocked from common phase locked clock
- Data word can be set independently for every channel
- For PRBS, each channel pattern can be independently seeded to give a per channel offset. Seeding modes synchronous, staggered and random
- Bit error generation on selected channel or all channels
- Fast trigger on pattern position (planned) or (1/4) of TX clock

RX

- Classic BERT functions – BERT receive compatible with TX modes
- Count of both 0 and 1 in error in BERT. Absolute count and ratio
- All results as summary and per channel
- Error count and ratio, start/stop and timed measurements
- Pattern loss alarm
- Fast trigger output on error (planned)

Unframed 10x10.3G BERT pattern configu ation screen
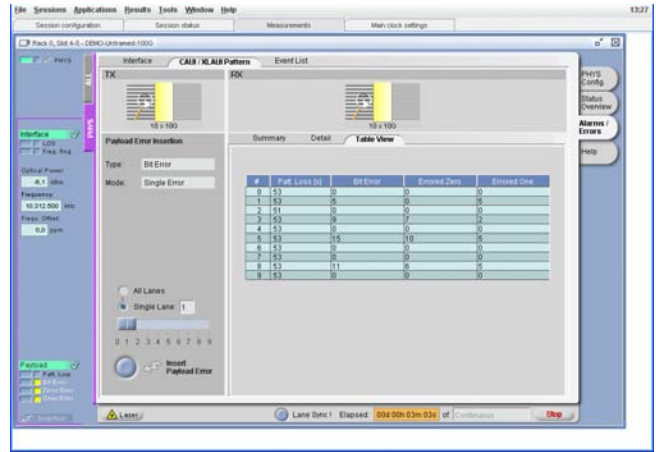
Unframed 10x10.3G BERT pattern tabular results screen

Unframed 20 channel BERT

- 20 channel BERT to give transparency through gearboxes
- Ten times two test patterns multiplexed onto one physical 10G lane giving a 20 channel PRBS on 10 physical lanes
- Supports PRBS (2^9, 2^{23} and 2^{31}) and digital word
- Summary and per channel results
- Features as unframed 10 channel BERT
- Supports per lambda mapping

Per lambda mapping feature

The individual lanes are mapped onto different lambdas via the action of the gearbox in the CFP module. This process is random at start up so you normally cannot generate an aggregated (per 25G lambda) BER to determine the full performance vital in the development and evaluation phase of CFP modules.

The 100G BERT offers a unique feature which allows the individual lanes to be grouped on a per-lambda basis greatly increasing the depth and breadth of testing that can be done over the link.
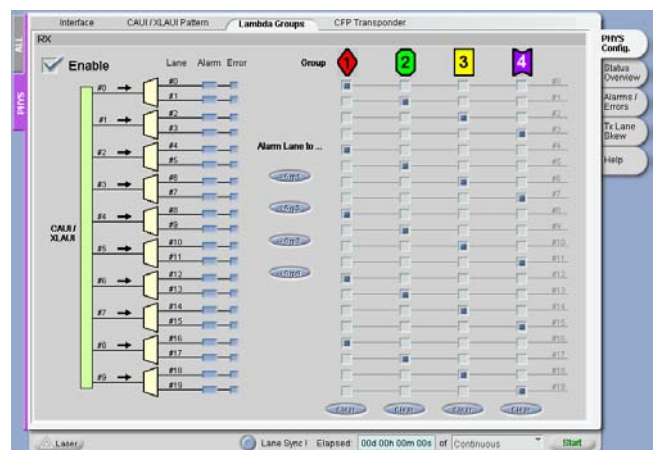
Lambda groups setup screen
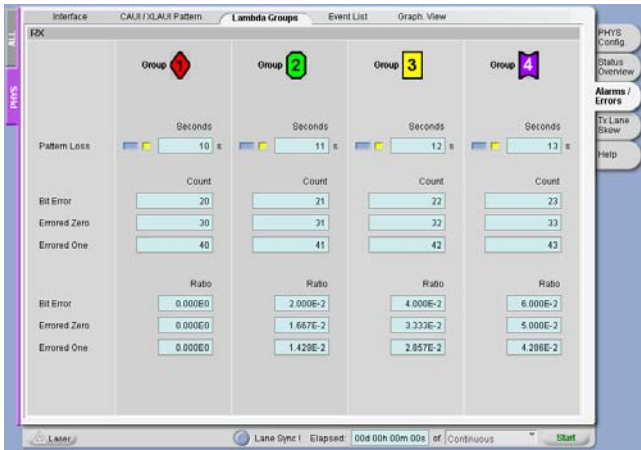
Lambda groups results screen

Block coded (framed) PCS layer BERT

- Generation and analysis of 64B/66B block coded data with embedded test pattern. Per virtual lane and aggregate test patterns supported
- Insertion and analysis of lane alignment markers for virtual lane identific tion and de-skewing
- Generation and analysis of BIP-8
- Virtual lane skew generation and measurement
- User programmable virtual lane mapping (lane rotation)
- Generation and analysis of all relevant PCS layer alarms and errors

Analysis and Generation of Virtual Lane Skew

- Lane delay generated to 32000 bits. Resolution 1 bit
- RX virtual lane skew tolerance 16000 bits
- Virtual lane skew measured to 16000 bits

### TX

- 2^9, 2^{23} and 2^{31} PRBS test patterns in per virtual lane mode
- Scrambled idle test pattern in aggregate mode
- Each lane clocked from common clock
- In virtual lane mode, each lane can be independently seeded to give a full range of possible PRBS relationships. Seeding modes synchronous, staggered and random are supported
- User programmable virtual lane mapping and virtual lane marker overwrite capability (user defined value) allows in-depth receiver de-skew and reassembly function testing
- Range of error insertions available for PCS sublayer (including loss of lock, loss of alignment etc). See "Basic Ethernet Features – PCS and reconciliation layers" for more details (only PCS sublayer alarms and errors are applicable)
- Large skew generation allows validation of PCS receiver under extreme conditions

RX

- RX BERT compatible with TX. Per virtual lane and aggregate mode
- Count of both 0 and 1 in error in per virtual lane mode. Absolute count and ratio
- Block error count and ratio in aggregate mode
- Summary and per virtual lane results
- Skew tolerance of 16000 bits
- Skew measurement to 16000 bits
- PCS layer alarms indicate alarm conditions. Analysis of all relevant PCS layer errors. See "Basic Ethernet Features – PCS and reconciliation layers" for more details (only PCS sublayer alarms and errors are applicable)

Lane Skew generation screen. Allows injection of static skew into each of the physical lanes.
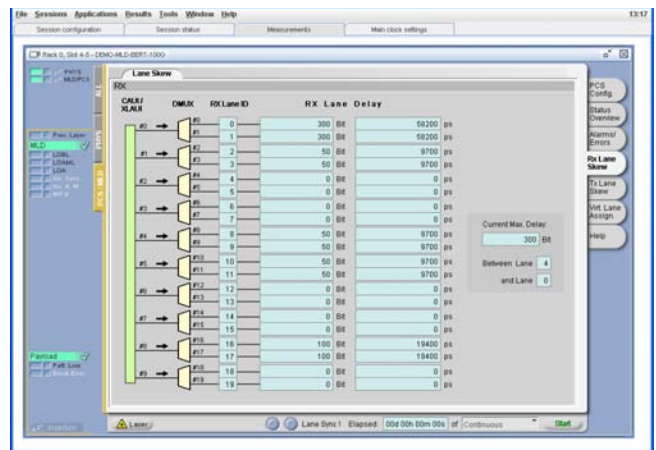
Lane Skew is monitored in both UI and ps
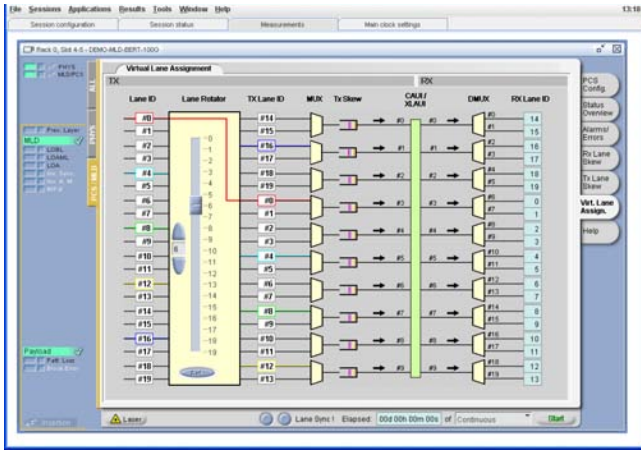
Lane rotator allows manual allocation and re-alignment of virtual lanes

Basic Ethernet Features

PCS and Reconciliation Layers

- Encoding and decoding of MAC frames as per IEEE 802.3ba
- State machines as per IEEE 802.3ba
- Virtual lane handling. User programmable lane skew generation (max. 32000 bits)
- RX lane de-skewing and skew measurement (max. 16000 bits)
- Programmable virtual lane mapping (lane rotation)
- 66B block statistics
- Generation and analysis of all relevant alarms and errors. Rate and burst generation capabilities. Selected lane and all lane modes where appropriate
- RX state machine testing supported by user definable syn . header and alignment marker
- PCS layer alarms: Loss of block lock (LOBL), loss of alignment marker (LOALM), loss of alignment (LOA). LOBL and LOALM event counters
- PCS layer errors: Invalid sync. header, invalid alignment marker, BIP-8 error
- PCS alarms/errors: High bit error rate (HI BER). Errored block and HI BER event counters
- Reconciliation sublayer: Link down, local fault, remote fault. Fault event counters

Basic MAC frame generation and analysis

- One MAC fl w for TX and RX supported
- Ethernet II frame type
- VLAN tagged frames. Single and double tagged
- BERT and JDSU test frame payload modes. Payload BERT supports BER testing, JDSU test frames support QoS measurement
- 100% bandwidth utilization on RX and TX
- Jumbo frame support (max. 10000 byte)
- Static and dynamic frame size (64 – 10000 bytes, increment, decrement, random)
- MAC error analysis and generation: Runt, oversized, FCS. Each supported as sngle, rate and burst generation modes
- PAUSE frame generation and analysis

- Frame statistics: Total bytes, total frames, good frames, errored frames, PAUSE frames, fil ered frames
- Bandwidth statistics: Total bandwidth, total utilization, filtered bandwidth, payload bandwidth
- Frame size statistics: Min. frame size, max. frame size, average frame size, frame size distribution

Payload BERT

- Payload is filled with a ^{31} PRBS test pattern. Pattern is analyzed for bit errors and pattern loss

JDSU test frames

- Frame payload is filled with a special JDSU test payload. This allows an in-depth analysis and measurement of various QoS parameters. Error related parameters: Frame loss, frame duplication, frame misinsertion, frame out of order. Results presented as rates and ratios
- Delay related parameters: Min. transfer delay, max. transfer delay, average transfer delay, transfer delay variation

Gap mode traffic generation

- Static and dynamic inter-packet gap (IPG)
- Fixed, increment, decrement and random IPG modes
- Minimum IPG is 8 bytes
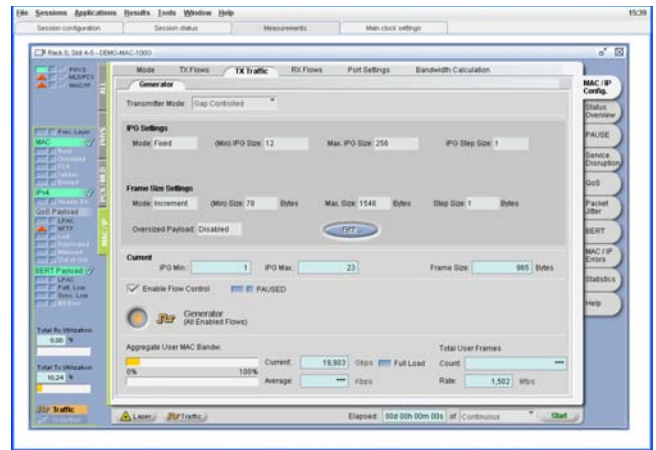
Gap mode traffic gen ator setup screen
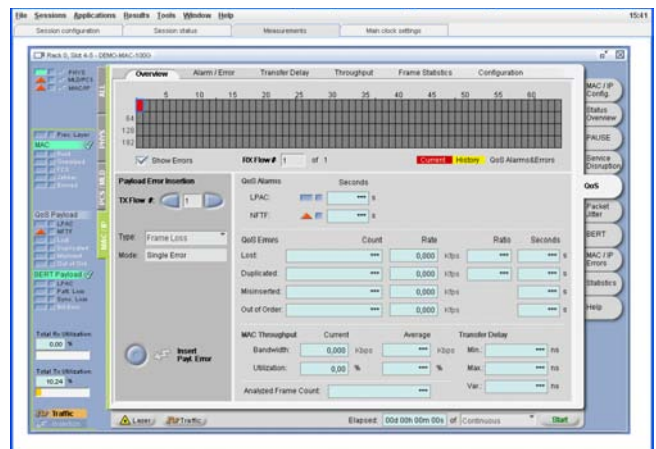
Enhanced Ethernet Features
(Planned for November 2009)

- Support for MPLS and IPv4
- Packet jitter measurement. Current, peak and average instantaneous packet jitter. Hit counter for packets exceeding a user defined th eshold
- Multi stream support with 256 fully independent streams. QoS and packet jitter measurement on all streams in parallel
- Service disruption measurement. Disruption measurement on all streams in parallel. Disruption duration, size (in frames) and type measured per stream
- Bandwidth mode traffic generation. Continuous and bursty traffic sources. User definable parameters for sustained bandwidth, peak bandwidth and burst size

40G applications

All the applications for 100G will also be available as 40G variants from unframed physical layer BERT through to Ethernet. The 40G option will enable all currently installed 100G options to be enabled for 40G applications. Initially this is supported over the CFP interface but will also be applicable over future transponder carry cards for QSFP or CXP as appropriate.

OTN OTU4 Features

The base 100G solution will support both unframed (111.8 Gb/s) and framed bulk payload for OTU4 based on suitable client optics (initially CFP) but later other options including the OIF MSA for 100G.

Basic analysis and error injection on the FEC is also supported.

OTN client board

This additional board is designed to deliver the power and future performance needed for full OTU4 traffic generation, analysis and validation down to the deep payload level.

Deeper OTU4 applications including

- Wrapper and dewrapper
- Add and drop
- Full FEC stress test and validation

Note: The exact content and features of each release will be published later. The features listed above are only provisional and may change due to the availability of technology and market demands.

Electrical Interface Adapter

This adapter is designed to meet the needs of developers who want to be able to develop and debug components and optics pre-CFP.

The native electrical adapter brings out the CAUI-like interface on a SMA pigtailed cable allowing connectivity to prototype boards and systems. No control or power signals are brought out.

Detail

Electrical signal accessed via high-density co-ax connector mounted on front panel of card. Pigtailed cables with the high-density co-ax connector on one end and SMA male connectors on the other are used to connect to the DUT.

Electrical signal	Differential with 20 RX and 20 TX lines (i.e. 10 pairs in each direction). An additional pair brings out a CFP reference clock (electrical lane speed 1/16 or 1/64, user selectable).
Data rates	Supports all unframed rates
Cable length	~30 cm

TX

Fixed level	Differential with ~800 mV swing
Nominal impedance	100 ohms (differential)

- All lanes have fixed timing and are driven by the same reference clock.
- A degree of electrical pre-emphasis is offered to compensate for the length of cable and PCB trace. The exact drive length is a complex factor of PCB material, layout and ASIC i/o characteristics.

RX

|	
Electrical signal	Differential
Sensitivity range	400 - 1200 mV
Nominal impedance	100 ohms (differential)

General

The electrical interface card is laboratory grade equipment and has no specific ESD protection so care must be taken while handling cables etc. Full ESD precautions must be taken.

The cable assembly is removable and can be replaced by the user.

This is a special request item. Consult factory.

CFP ⇔ CFP active cable

The active cable allows the ONT to act as a 'golden transponder'. One end of the cable plugs into the CFP slot on the ONT transponder carry card while the other end, also a CFP module, can plug into a board under test acting as a reference transponder. The active cable is approximately 3m long and is based on well proven active cable technology to give high signal integrity. Application include turn up of CFP interfaces in line cards and validation and verification of CFP optical modules.
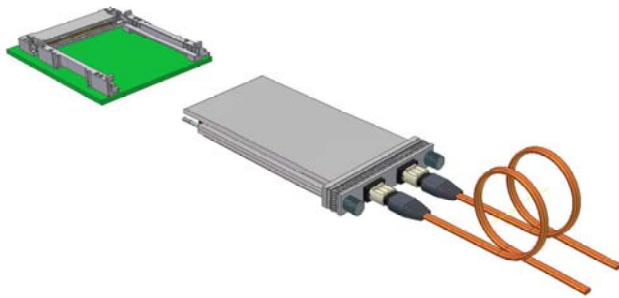
General

Active cable with CFP MSA 1.0 compliant modules at each end.

Interconnect based on multi-mode optical fibre with pluggable connectors.

No MDIO command I/O response.

Power dissipation	Approximately 7.5 W per module.
Cable length	~3 m
Operating temperature range	0°C - 70°C

Orderable packages

100G Test Solution Base Unit with CFP Interface

Includes base unit and CFP transponder carry card.

Applications for 100GE L2 and Ethernet Connectivity

PCS layer applications, Ethernet connectivity and validation to layer 3.

100G Hardware Validation – Option (requires 100G base unit)

Additional hardware and software applications for detailed physical layer validation and troubleshooting.

Includes enhanced trigger I/O capabilities, MDIO interface, CFP ⇔ CFP active cable

Enhanced applications include unframed BERT, per Lambda BERT, PCS layer skew stress test, electrical layer margin test.

Note: This is a factory upgrade

100G OTU4 Bulk – Option (requires 100G base unit)

Additional applications for generation of OTU4 rate signals (both unframed – no payload) and framed with basic pseudo 100GE payload and FEC error injection and test.

40GE option (requires 100G base unit)

Enables 40G line rate applications with all appropriate enabled options such as Ethernet, hardware validation, OTN etc.

JDSU 40GE/100GE/OTU4 test system

MDIO Front panel connector

The MDIO interface is brought out on an RJ jack on the front panel. Normally the test application controls the transponder directly but in early phases (especially when transponder firmware is under development) the 40GE/100GE/OTU4 solution allows external control of the MDIO interface.

This can be used during the development and turn up phase to allow full control over the transponder.

Connector assignment for transponder management interface (MDIO)

#	Signal	Pin	Dir	Level	"H"	"L"	Pull-up/ down[1]	Additional Info
1	MDIO	3	I/O	1,2 V LVCMOS	-	-	Up (470 Ohm)	Management Data
2	MDC	1	I/O	1,2 V LVCMOS	-	-	Up (470 Ohm)	Management Clock
3	MOD_RSTn	4	I	3,3V LVCMOS	Enable	Reset	Up	Module reset
4	MOD_LOPWR	8	I	3,3V LVCMOS	Deselect	Enable	Up	Module low power mode
5	MOD_ABS	7	O	3,3V LVCMOS	Absent	Present	N/A	Module absent ("No CFP")
6	GLB_ALRM	5	O	3,3V LVCMOS	Alarm	No alarm	N/A	Global alarm
7	GND	2	N/A	N/A	N/A	N/A	N/A	Ground
8	GND	6	N/A	N/A	N/A	N/A	N/A	Ground

[1] On transponder board